REMARKS

The claims are claims 1 to 4.

Claims 1 to 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al U.S. Patent 4,463,443 and Steinmetz et al U.S. Patent 5,809,521.

Claims 1 recites subject matter not made obvious by the combination of Frankel et al and Steinmetz et al. Claim 1 recites a copy/access controller "operable to copy data from said first buffer to said second buffer when said first buffer is substantially full" and "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." These limitations are not made obvious by the combination of Frankel et al and Steinmetz et al. The FINAL REJECTION cites: input data register 10 of Frankel et al as making obvious the claimed first buffer; output data register 14 of Frankel et al as making obvious the recited second buffer; and the elements RAM 16, RAM address counters 16a, RAM input holding register 18, RAM output holding register 20 and write and read sequence generator and control logic of Frankel et al as making obvious the recite copy/access controller. Presumably the recited first component is the apparatus supplying data to input data register 10 and the recited second component is the apparatus receiving data form output data register 14. The FINAL REJECTION states at page 3, lines 8 to 11:

> "Frankel fails to explicitly teach the prompting of a second component to access the second buffer when the data is copied from the first buffer. However, it was notoriously well known in the art at the time of invention to use signal to prompt buffer connected devices to read and write data to and from the buffer."

The Applicants agree with this statement of the Examiner. Frankel et at states at column 3, lines 59 to 63:

> "In a similar manner, the data is output from the buffer at the output data register 14 synchronously with the output data clock. When the output data register 14 is empty, data in the RAM output register 20 is transferred to it."

This portion of Frankel et al teaches continuous output of data from output data register 14 to the second component not shown. This portion of Frankel et al fails to teach prompting this second component "to access said second buffer when said data is copied from said first buffer" as recited in claim 1. Instead, this language strongly implies that access by the second component to data stored in the second buffer does not require any such prompting. The Applicants submit that the above quoted language of claim 1 requires more than merely writing to the output shift register. This language requires generation of a prompt signal by the copy/access controller to initiate reading data by the second component. The Applicants submit this limitation is not inherent in the mere writing of data to the buffer. The FINAL REJECTION cites element 16 and nEMPTY signal illustrated in Figure 1b and column 3, line 40 to column 4, line 5 of the secondary reference Steinmetz et al as making obvious this subject matter. Steinmetz et al states at column 3, line 62 to column 4, line 1 (within the section cited by the Examiner):

> "Each FIFO memory is cascaded by connecting the 'not empty' (nEMPTY) signal of one FIFO to the write terminal of the succeeding FIFO, the 'not full' (nFULL) signal to the read terminal of the preceding FIFO and the data output terminal (DATAOUT) of one FIFO to the data input (DATAIN) terminal of the succeeding FIFO."

The Applicant assumes that the Examiner's position is that the nEMPTY signal of FIFO 16 causes the not illustrated receiving system to access data for read out from FIFO 16. This teaching of Steinmetz et al differs from the above quoted language of claim 1 because there is not a single structure (the claimed copy/access controller) which both copies data to the second buffer and prompts the second component to access the second buffer. This subject matter is illustrated at element 24 in Figure 4 of this application. Note that in Steinmetz et al writing to FIFO 16 is caused by the nEMPTY signal of FIFO 14 coupled to the WRITE input of FIFO 16. However, FIFO 14 does not prompt the second component to access this data in FIFO 16 are required by claim 1. Instead, the nEMPTY signal of FIFO 16 makes this prompt. In particular, there is no disclosure in Steinmetz et al that the nEMPTY signal of a FIFO is generated by the same component that copies data into the second buffer. The FINAL REJECTION states at page 2, lines 6 to 11:

> "Applicant also argues that Stienmetz is differentiated because of a lack of a single structure. This argument also does not address the rejection as stated. The teaching of a single structure is clearly shown in the primary reference, Frankel. If the teaching of a single structure was found in Steinmetz, there would have been no need for any of the teachings of Frankel, and Stienmetz could have been used in an anticipation rejection."

The Applicant respectfully submits that neither Frankel et al nor Steinmetz et al teach the recited copy/access controller. Particularly, neither Frankel et al nor Steinmetz et al teach the recited copy/access controller which both operates "to copy data from said first buffer to said second buffer when said first buffer is substantially full" and "to prompt said second component to access said second buffer when said data is copied from said first

buffer." Accordingly, claim 1 is allowable over the combination of Frankel et al and Steinmetz et al.

Claims 2 to 4 are allowable by dependence upon respective allowable base claim 1.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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